Inventor:

Luan C. Tran

Title:

Methods of Forming Semiconductor Constructions

Assignee:

Micron Technology, Inc.

## **INFORMATION DISCLOSURE STATEMENT**

## PURSUANT TO 37 C.F.R. §§ 1.56, 1.97 AND 1.98

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a divisional application of co-pending application Serial No. 10/364,054, filed February 10, 2003. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. § 1.98(d) and MPEP § 609(2).

Citation of these references is respectfully requested.

Respectfully submitted,

Dated:

Rv.

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Taylor,

Form PTO-144	19				ATTY. DOCKET NO. MI22-2356				priority SERIAL NO. 10/364,054				
LIST OF ART CITED I (Use several sheets							APPLICANT Luan C. Tran						
							priority FILING DATE February 10, 2003			priority GROUP 2812			
					U.S. PATENT DOCUMENTS	;							
*Examiner Initial		Document Number		Date	Name	Name			ass Subclass		Filing Date If Appropriate		
	AA	6,458,666 B2		10-2002	Wasshuber								
	AB	6,444,	,548 B2	09-2002	Divakaruni et al.								
	AC	3,886,	,003	05-1975	Takagi et al.								
	AD	4,366,338		12-1982	Turner et al.								
	AE	6,008,115		12-1999	Jung								
	AF	6,506,647 B2		01-2003	Kuroda et al.	Curoda et al.							
	AG	US2001/0036713A1		11-01-2001	Rodder et al.						July 5, 2001		
	AH	US2002/0034865A1		03-21-2002	Umimoto et al.						Nov. 30, 2001		
	AI	09/876	6,722		Scott						June 6, 2001		
	AJ	10/133,193			McQueen et al.						April 26, 2002		
	AK												
1	AL												
		,			FOREIGN PATENT DOCUMEN	NTS			·				
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	AP	L	01	HER REFEREN	ICES (including Author, Title, Date	e. P	Pertinent Pages, Etc.)		L			L	
	AQ		r		echnology with 193 nm Lithograp	_	<del></del>	igh Performa	ance Ap	pplication	ons", IEDM,	pgs. 563-	
	300, Арті 2000.												
	AR	Yeh et al., "Optimum Halo Structure for Sub-0.1 μm CMOSFETs", 1EEE Transactions on Electronic Devices, Vol. 48, No. 10, October 200 pgs. 2357-2362.											
	AS		Bouillon et al., "Re-examination of Indium implantation for a low power 0.1 μm technology", IDEM, pgs. 897-900, 1995 (year is sufficient so that date is not in issue).										
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EXAMINER			L		DATE CONSIDER	REI	D						
*EXAMINER: Include copy o	*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered.  Include copy of this form with next communication to applicant.												